Quantum Computing-Based Integration of Modulo 2n+1 Adders for Edge Detection

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Abstract

The rapid advancements in quantum computing have opened new possibilities for optimizing complex computational tasks, including image processing and edge detection. This Project explores the integration of Modulo 2^N+1 Adders in a quantum computing environment for efficient edge detection, utilizing key quantum gates such as the CNOT (Controlled NOT Gate) and Toffoli Gate (Controlled-Controlled NOT Gate). Traditional edge detection algorithms, such as Sobel and Canny, often suffer from high computational demands, limiting their real-time or resource-constrained applications. By leveraging the inherent parallelism and superposition properties of quantum systems, the proposed approach integrates Modulo 2^N+1 Adders, which help reduce the computational complexity of arithmetic operations involved in edge detection tasks. The CNOT and Toffoli gates play a crucial role in the quantum circuit design, enabling the efficient implementation of modulo arithmetic and enhancing the speed and accuracy of edge detection. These quantum gates, which are fundamental in constructing quantum circuits, enable a significant reduction in the time complexity of detecting edges in images. The proposed system provides a promising solution for applications in computer vision, medical imaging, and real-time video processing. This study demonstrates how the integration of quantum gates and Modulo 2^N+1 adders can lead to the optimization of edge detection algorithms, offering scalable and efficient solutions that surpass classical computing methods.

Keywords*: Quantum Computing, Edge Detection, CNOT Gates, Toffoli Gates.*

INTRODUCTION

Quantum computing has emerged as a revolutionary field with the potential to solve complex computational problems using qubits, superposition, and entanglement. One significant area where quantum computing can make an impact is image processing, particularly in edge detection. Traditional edge detection algorithms, including Sobel and Canny, often face limitations in terms of computational speed and accuracy. Quantum computing offers a novel approach by leveraging Modulo 2N+1 Adders, optimizing modulo arithmetic operations to reduce computational complexity.

Modulo 2N+1 Adders play a pivotal role in performing arithmetic operations efficiently. These adders, when implemented using quantum circuits with Controlled-NOT (CNOT) and Toffoli gates, offer significant improvements in speed and accuracy. Compared to classical methods, quantum-based edge detection algorithms provide faster computation with reduced power consumption, making them ideal for real-time applications in computer vision and medical imaging. Furthermore, in portable and battery-operated devices, the Residue Number System (RNS) proves beneficial due to its low power consumption and parallel processing capability. Despite its advantages, the reverse conversion process in RNS remains a challenge due to its complexity and time-consuming nature. Addressing this, researchers have introduced parallel-prefix adders and optimized hardware components to design faster reverse converters. This study focuses on leveraging the advantages of quantum computing to enhance edge detection using Modulo 2N+1 Adders. It aims to evaluate the computational speed, accuracy, and efficiency of quantum-based edge detection compared to traditional approaches.

LITERATURE SURVEY

The Quantum Cybersecurity Threat May Arrive Sooner Than You Think by P. Ford (2023) discusses the emerging threats posed by quantum computing to traditional cybersecurity systems. While this study focuses on the risks associated with quantum technology, it emphasizes the urgency of quantum-resistant encryption without addressing practical implementation details. Quantum Technology for Military Applications by M. Krelina (2021) explores various military applications of quantum technology, including secure communication and quantum radar. Although insightful, the study is predominantly theoretical and lacks practical validation, limiting its applicability to real-world scenarios. Advances in the Quantum Internet by L. Gyongyosi and S. Imre (2022) reviews the principles and potential applications of the quantum internet. The study outlines challenges in implementing large-scale quantum networks, emphasizing the need for further hardware development. Dynamics of Entangled Networks of the Quantum Internet by L. Gyongyosi (2020) investigates the stability of entangled quantum networks. While the research contributes to the understanding of network dynamics, it remains theoretical with limited experimental data. Quantum Internet—Applications, Functionalities, Enabling Technologies, Challenges, and Research Directions by A. Singh et al. (2021) presents a comprehensive overview of the quantum internet, highlighting its potential applications and research challenges. However, it lacks in-depth technical implementation details. Design of Reverse Converter Using Parallel Prefix Adders and CRT by J. Brindha Devi and G. Rohinipriya (2015) proposes an efficient reverse converter design for the RNS using Parallel Prefix Adders. The study addresses the power consumption challenges and provides a trade-off between speed and area by employing optimized hardware components. Adder-Based Residue to Binary Number Converters for (2N-1, 2N, 2N+1) by Y. Wang, X. Song, M. Aboulhamid, and H. Shen (2002) presents novel residue-to-binary converters using adders. The study demonstrates improved speed and reduced hardware requirements compared to previous designs, contributing significantly to converter design advancements.

This research builds upon these foundational studies by applying quantum computing concepts to enhance edge detection algorithms, aiming to achieve higher efficiency, lower power consumption, and improved accuracy compared to classical methods.

DATA AND METHODOLOGY

The proposed system leverages quantum computing to perform efficient edge detection in digital images using quantum gates such as CNOT and Toffoli to implement logic operations and arithmetic functions. Modulo 2N+1 Adders are integrated into the quantum circuit to optimize complex calculations, reducing the computational burden and enhancing processing speed. By employing these quantum gates, key operations like arithmetic calculations and logic functions essential for edge detection are performed efficiently, resulting in improved accuracy and reduced complexity compared to traditional methods like Sobel and Canny edge detection. The quantum-based system is designed for scalability, making it suitable for real-time applications in computer vision, medical imaging, and video processing.

The methodology involves the use of quantum modulo arithmetic operations, where a Modulo (2N + 1) Adder computes gradient magnitudes and directions with high precision. Quantum Multipliers, implemented using Toffoli gates and modular arithmetic, further optimize the gradient calculations. The system utilizes a thresholding mechanism to generate a binary edge map using quantum comparator circuits. After processing, the quantum states representing the edge map are measured and converted back to classical data for accurate edge detection output.

In contrast to traditional approaches, Sobel edge detection is employed as a benchmark for comparison. Sobel's first-order derivative operator computes the gradient magnitude and direction using convolution masks applied to the image. This method involves applying both horizontal and vertical masks to capture edge information. Although the Sobel operator offers advantages such as noise reduction and edge enhancement, the proposed quantum-based system outperforms it by significantly reducing computational time and enhancing edge detection accuracy.

The proposed system also incorporates modules like quantum-based edge detection using gates, buffer management, and parallel prefix adder-based approximation stages. The Approximate Parallel Prefix Adder (AXPPA) proposal enables controlled bit-level approximations and optimized prefix computations for enhanced resource efficiency. This modular approach ensures flexibility in adjusting computational accuracy to meet specific application requirements, making it ideal for various fields including signal processing, image recognition, and machine learning accelerators.

Additionally, the system's use of quantum arithmetic operations ensures minimal latency and optimal energy efficiency, which is crucial for large-scale image and video processing tasks. Quantum thresholding circuits dynamically adapt to variations in pixel intensity, providing precise edge map generation. Furthermore, integrating buffer circuits helps manage data flow efficiently within the quantum architecture, reducing memory access delays. These advantages make the system robust and capable of handling real-time image processing demands in surveillance systems, autonomous vehicles, and medical diagnostic tools.

The accuracy of the proposed system is further validated through extensive simulations and comparative analysis with traditional methods. Performance metrics such as edge detection accuracy, computational time, and resource utilization are analyzed to demonstrate the system's superiority. The proposed quantum-based approach exhibits significantly lower error rates and faster processing times compared to conventional Sobel-based detection, making it a suitable candidate for next-generation image processing applications.

PROPOSED SYTEM

The system leverages quantum computing to perform efficient edge detection in digital images, using quantum gates such as CNOT and Toffoli to implement logic operations and arithmetic functions required for image processing. Modulo 2N+1 Adders are integrated into the quantum circuit to perform efficient modulo arithmetic operations. These adders help optimize the complex calculations involved in edge detection, reducing the computational burden and speeding up the process. The system utilizes CNOT (Controlled NOT) and Toffoli (Controlled-Controlled NOT) gates to perform key operations such as arithmetic calculations and logic functions necessary for edge detection, significantly enhancing the processing speed. The proposed quantum-based system is designed to outperform traditional image processing techniques like Sobel and Canny edge detection by offering faster computation, reduced complexity, and improved accuracy in detecting edges. The system is designed to be scalable and applicable to real-time image processing tasks, making it suitable for applications in computer vision, medical imaging, and video processing, where efficiency and speed are crucial.

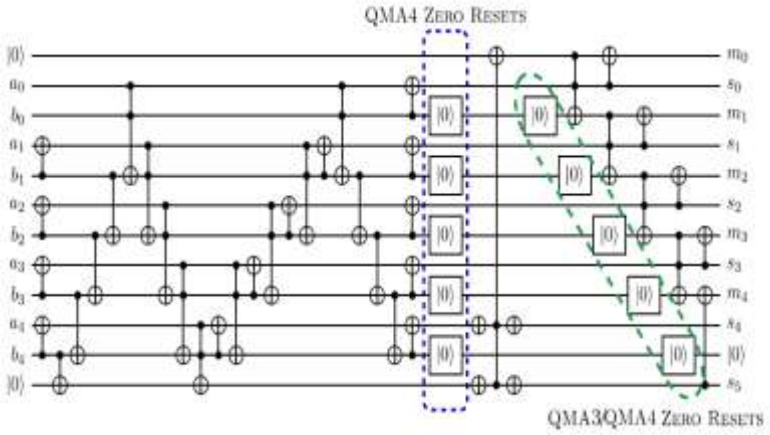


Figure 1 Block Diagram of Gates

Edge Detection Using Proposed Adder

The proposed edge detection algorithm leverages a Modular Adder implemented using quantum computing principles. The process begins with MATLAB converting the input image into text-based data. This textual representation is then processed using the Modular Adder to detect significant changes in pixel intensity, representing. image edges.

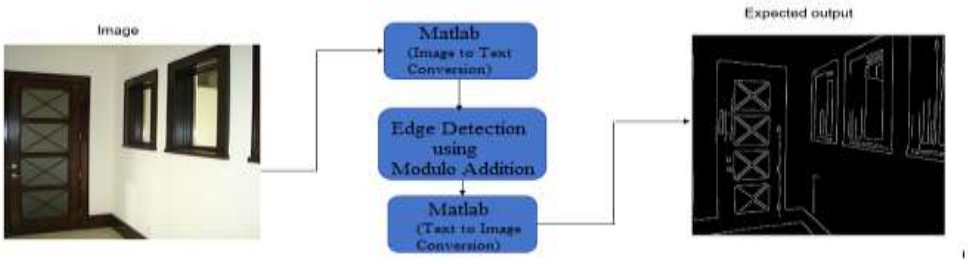


Image
Matlab
(Image to Text Conversion)
Edge Detection using Modulo Addition
Matlab
(Text to Image Conversion)
Expected output

Figure 2 Edge Detection Using Proposed Adder

The Modular Adder utilizes a combination of quantum gates, including Hadamard, CNOT, and Toffoli gates, to perform addition operations in the quantum domain. These operations identify pixel intensity variations by examining the differences between adjacent pixel values. The algorithm applies logical operations to extract edges, ensuring sharp boundary detection. Once the edge detection process is completed using the Modular Adder, the output is converted back into a text representation. MATLAB then converts this text-based data into a visual image, representing the detected edges. This quantum-based approach ensures enhanced accuracy and faster processing compared to traditional edge detection methods. The effectiveness of the proposed adder is evident in its ability to capture fine edge details while reducing noise and artifacts. The results demonstrate improved edge clarity and precision, validating the advantages of using quantum computing for image processing applications.

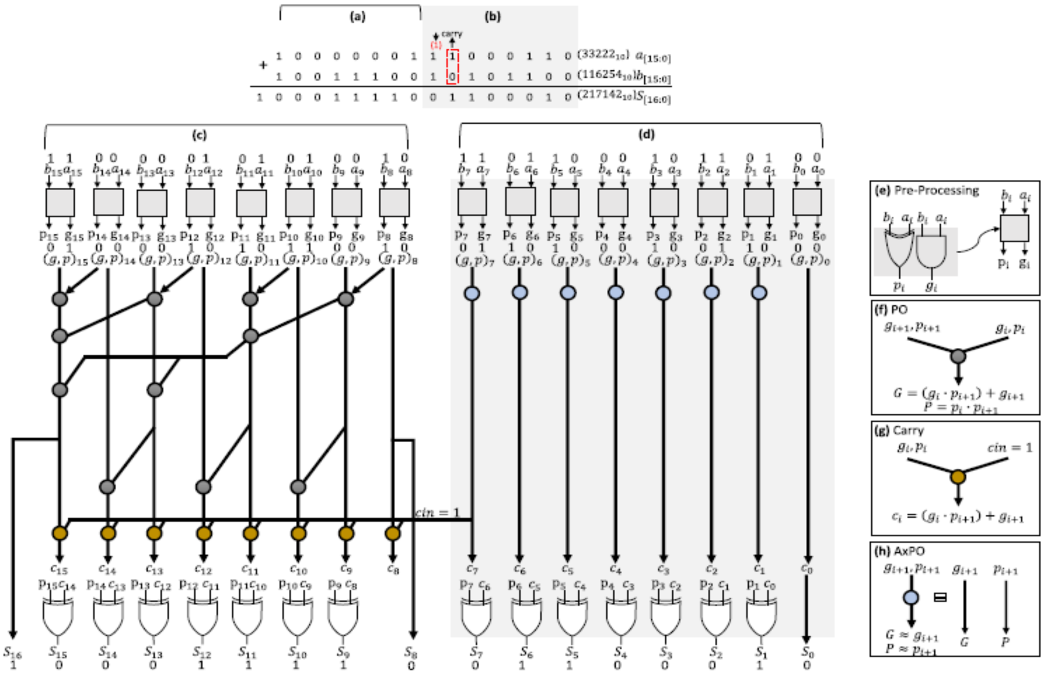


Figure 3 8-Bit Identity Comparator

Propsoed System Applications

Signal Processing: Real-time processing of signals in communication systems, where the speed and energy efficiency of the approximate parallel prefix adder can enhance tasks like filtering, modulation, and demodulation.

Image and Video Processing: Accelerating real-time image and video processing applications, such as object recognition and tracking, where the algorithm's optimized resource usage is beneficial for handling large datasets.

Embedded Systems: Integration into embedded systems for real-time applications like robotics, where the algorithm's efficiency contributes to faster decision-making and precise control.

Digital Signal Processors (DSP): Implementation in DSPs for real-time audio processing applications, taking advantage of the algorithm's ability to balance accuracy and resource efficiency in computationally intensive tasks.

Machine Learning Accelerators: Deployment in hardware accelerators for machine learning algorithms, leveraging the optimized architecture to enhance the speed and efficiency of approximate computations in neural networks.

Cryptographic Systems: Integration into cryptographic systems for real-time encryption and decryption, benefiting from the algorithm's capacity to handle complex arithmetic operations efficiently.

Quantum Modulo-Based Edge Detection

The proposed system employs quantum computing principles to achieve efficient edge detection in digital images. It integrates quantum logic gates, including CNOT and Toffoli gates, with modulo arithmetic operations using specially designed quantum-based adders and multipliers. These components are implemented to enhance processing speed, improve accuracy, and minimize computational complexity compared to traditional edge detection methods. Image preprocessing is carried out using MATLAB, where input images are converted to quantum states using suitable encoding schemes such as amplitude encoding or basis encoding. This encoding enables pixel intensity values to be represented as quantum states, which are then processed using quantum circuits.

In the edge detection phase, a Modulo (2N + 1) Adder is used to efficiently manage modular arithmetic operations.

$$\text{Modulo Sum } = \begin{cases} a+b & \text{if } (a+b) < 2^N+1 \\ 0 & \text{if } (a+b) = 2^N+1 \\ (a+b)\text{mod}(2^N+1) & \text{if } (a+b) > 2^N+1 \end{cases}$$

This quantum adder calculates gradient magnitudes and directions with high precision while maintaining a minimal gate overhead. The CNOT and Toffoli gates facilitate logical operations for detecting pixel intensity variations, ensuring accurate edge identification. A dedicated quantum multiplier computes the gradient magnitudes and directions using optimized Toffoli gates and modular arithmetic, reducing complexity and increasing processing speed.

Following the gradient calculation, quantum-based thresholding is applied using a comparator circuit. This process determines whether a pixel is part of an edge based on a dynamically calculated threshold value. The binary edge map generated from this operation represents edge pixels as 1 and non-edge pixels as 0. Post-processing is then performed to refine the results. The quantum states representing the processed edge map are measured and converted back to classical data, reconstructing the edge-detected image using MATLAB. This ensures that the final output accurately captures and highlights the edge details.

Additional components of the system include digital buffers, which serve to isolate the input from the output while maintaining signal integrity. Parallel prefix operators denoted by ¢ as follows:

$$(G'', P'') \text{¢} (G', P') = (G''+G'\cdot P'', P'\cdot P'')$$

where P" and P' indicate the propagations, G" and G' indicate the generations. The fundamental carry operator is represented as Figure 4.

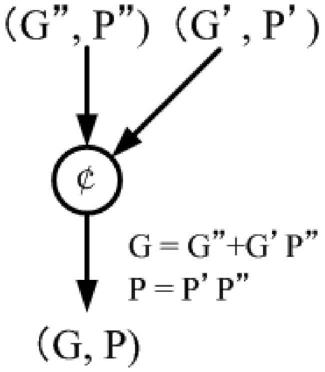


Figure 4 Carry Operator

A parallel prefix adder can be represented as a parallel prefix graph consisting of carry operator nodes. Figure shows the parallel prefix graph of a Ladner-Fischer adder. This adder structure has minimum logic depth, but has large fan-out requirement up to n/2.

Proposed AXPPA

The prefix computing in a PPA is composed of sets of Pos. The AxPPA proposals exploit approximations in the logic of part of its POs. The number of approximate POs can be configurable at design time to adjust the desired exactness of the AxPPA. Fig. shows that our AxPO uses just wires to process the prefix computing, connecting the preprocessing to the postprocessing. The computation of POs is described the computation of AxPOs.

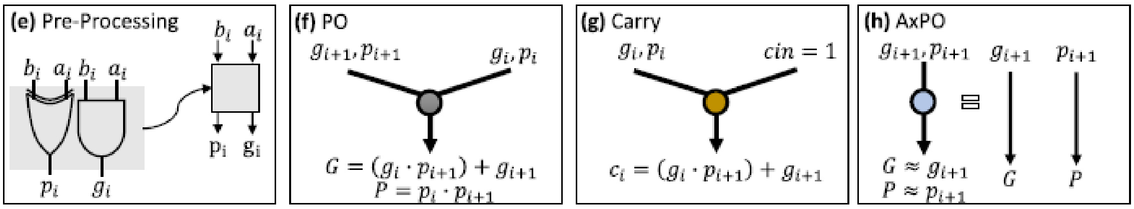


Figure 5 Pre-Processing, PO, Carry and AxPO

The Sobel edge detection algorithm is also integrated into the proposed system for comparison.

$$G_x = \sum_{i=-1}^{1} \sum_{j=-1}^{1} K_x(i,j) \cdot I(i,j)$$

$$G_y = \sum_{j=-1}^{1} K_y(i,j) \cdot I(i,j)$$

$$G = \sqrt{G_x^2 + G_y^2}$$

Sobel operators, known for their robustness against noise, apply horizontal and vertical convolution masks to detect edges. The system reads input image data using MATLAB, applies the Sobel masks, and calculates the gradient magnitudes using convolution. Afterward, the gradient values are compared against a threshold to determine true edges.

$$E(x,y) = \begin{cases} 1 & \text{if } G(x,y) \geq T \\ 0 & \text{if } G(x,y) < T \end{cases}$$

By combining quantum computation with traditional Sobel edge detection, the system ensures comprehensive and accurate edge detection in digital images. The overall design offers significant advantages in terms of low power consumption, high throughput, and enhanced noise tolerance, making it ideal for real-time applications in fields like computer vision, deep learning, and natural language understanding.

Sobel Edge Detection

Algorithm for Sobel Edge Detection The Sobel Edge Detection Operator is 3×3 spatial mask. It is based on first derivative based operation. The Sobel masks are defined as:

$$H1 = \begin{array}{ccc} -1 & -2 & -1 \\ 0 & 0 & 0 \\ 1 & 2 & 1 \end{array} \qquad H2 = \begin{array}{ccc} -1 & 0 & 1 \\ -2 & 0 & 2 \\ -1 & 0 & 1 \end{array}$$

Suppose the pixel value of a 3×3 sub-window of an image is as shown as in Table 1

Table 1 The Pixel Intensity Values of a 3×3 Sub-window of an Image

D0	D1	D2
D3	D4	D5
D6	D7	D8

Applying the Sobel mask on the sub-window of Table 1 yields

$$G_x = (D6 + 2\times D7 + D8) - (D0 + 2\times D1 + D2)$$
$$= f1 - f2 \text{ Where, } \quad f1 = (D6 + 2\times D7 + D8) \text{and } f2 = (D0 + 2\times D1 + D2)$$

$$G_y = (D2 + 2\times D5 + D8) - (D0 + 2\times D3 + D6)$$
$$= f3 - f4 \text{ Where, } f3 = (D2 + 2\times D5 + D8) \text{and } \; f4 = (D0 + 2\times D3 + D6)$$

Module Explanation

Reading Image

Sobel operator is used to detect edges of the test images used. This procedure is applied on more than one test image as shown in Fig. 6. Firstly the image data is read as an array with the dimension of image size. The number of elements of this array is calculated in order to resize the array of image to another array. The resizing that be used is (256×256) in MATLAB program.

Figure 6 Test Images

Applying the Convolution Mask I and J on the Input Image

The horizontal template and vertical template shown in Fig 6 above are used to get convolution with input image by using equations. The result matrix after this operation is got the same size of two gradients Matrix Gx and Gy as the original image as shown in Fig 7

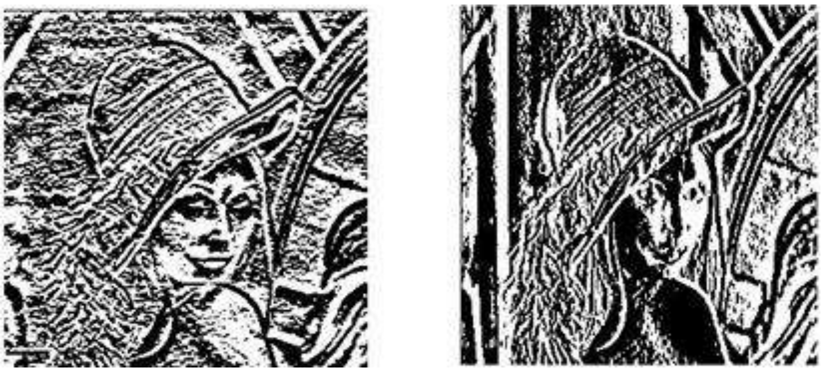


Figure 7 Convolution Mask I and J on the Input Image

Determine the Gradient Magnitude by Computing

The gradient magnitude is determent by squaring the pixels values of each filtered image, Then Adding of the two results and computing their root to get the total gradient value (Gr) are done.

Sobel Edge Detetor Operator

Sobel Edge Detection, there are two masks, one mask identifies the horizontal edges and the other mask identifies the vertical edges. Each of the masks has the effect of calculating the gradient in both vertical and horizontal direction. These Sobel masks are convolved with smoothed image and giving gradients in i and j directions is given by

Gi=Gx*F(i,j) and Gj=Gy*F(i,j)

Sobel masks are showing in Table 2

Table 2 Sobel Masks

-1	-2	-1
0	0	0
1	2	1

-1	0	1
-2	0	2
-1	0	1

Compare the Gradient Magnitude with Threshold Value and Find True Edges

Finally, the edges can be detected by applying the threshold by using equation (5) to the total gradient (Gr). If (Gr) is greater than the threshold, then pixel should be identified an edge as shown in Figure . Else it's not identified as an edge. This Edge Detection logic is made by Schostic Logic Circuit.

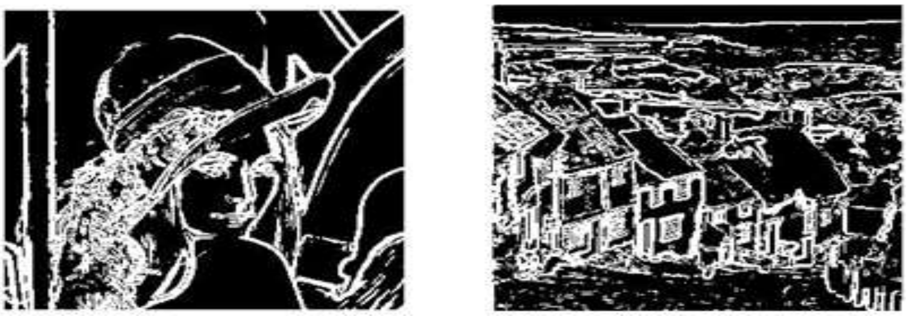


Figure 8 Output obtained by Schostic Logic Circuit

Proposed System Sobel Edge Detection Block Diagram

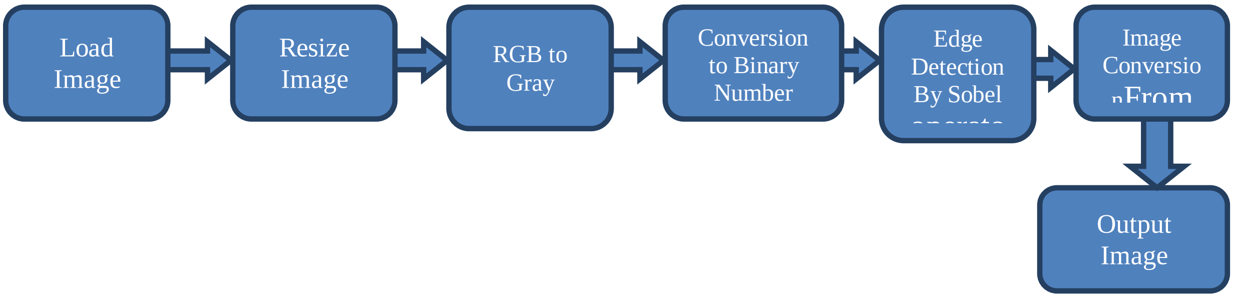


Figure 9 Main Block Diagram

The given flowchart represents an edge detection process using the Sobel operator, with additional steps for optimization and decision-making. The process begins with aligning the input image, ensuring that the image is correctly formatted for further processing. The aligned image is then subjected to multiplication using the Sobel operator, which detects edges by computing the gradient magnitude based on intensity differences.

Following this, the output from the Sobel operation is passed through a compressor, which likely reduces data complexity or refines the edge detection results. Next, a threshold voltage is introduced as a reference, which helps determine significant edges. Both the compressed Sobel output and the threshold voltage are fed into a comparator, which evaluates the gradient strength against the threshold.

Finally, the output (0,1) represents a binary decision, where 0 indicates no edge, and 1 signifies an edge detected. This structured approach ensures efficient edge detection with possible applications in image processing, object recognition, and computer vision tasks.

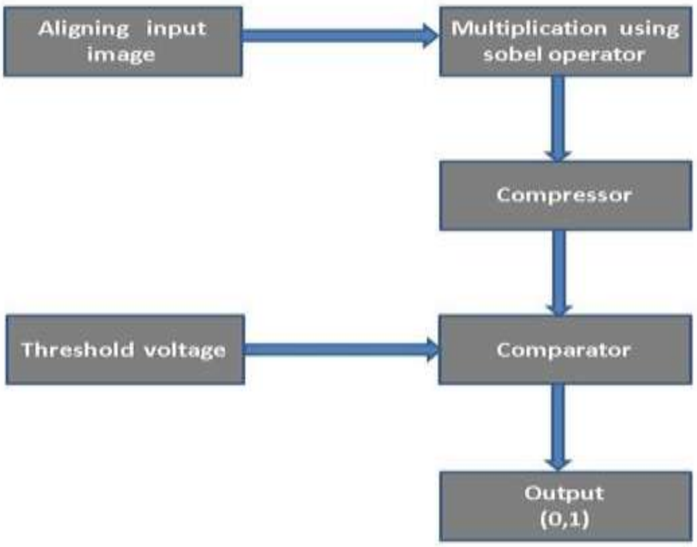


Figure 10 Edge Detection Process Using Sobel Operator

Proposed System Flow

Process Flow of RGB to Binary Image Conversion (MATLAB Part)

The given flowchart outlines the systematic process of converting a JPG image into a binary representation, which is fundamental for various image processing applications. The process begins with acquiring a JPG image as the input. Next, the image undergoes a transformation from RGB to grayscale, simplifying it by reducing the color channels while retaining the intensity information. Once converted to grayscale, a thresholding technique is applied to transform the image into a binary format, where pixel intensities are classified as either black (0) or white (1). This binary representation makes further computational analysis more efficient. Finally, the processed binary image is stored as a text file, ensuring ease of retrieval and manipulation for subsequent image processing tasks. This method plays a crucial role in applications such as edge detection, pattern recognition, and other digital image processing techniques where simplified image representation enhances computational efficiency.

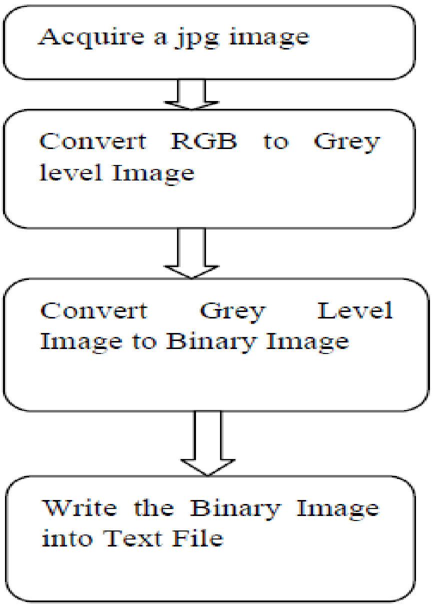

Acquire a jpg image
Convert RGB to Grey level Image
Convert Grey Level Image to Binary Image
Write the Binary Image into Text File

Figure 11 Process Flow of RGB to Binary Image Conversion (MATLAB Part)

VLSI Part (using Modelsim)

The flowchart describes the step-by-step process of edge detection using a binary image stored in a text file, a crucial technique in image processing applications such as object recognition and computer vision. The process begins with reading the binary image into memory, where it is prepared for further analysis. Once loaded, the system performs edge detection by computing gradients in both the horizontal and vertical directions (x and y gradients), identifying significant changes in pixel intensity that indicate the presence of edges.

Next, the detected horizontal and vertical edge components are combined to calculate the overall edge magnitude, which enhances the accuracy and clarity of edge detection. This step ensures that edges are well-defined and more distinguishable from the background. Finally, the edge-detected image undergoes synthesis and simulation, where the results are evaluated to verify the effectiveness of the process. The final design summary is checked, ensuring that the edge detection algorithm performs efficiently and meets the required accuracy standards. This method plays a critical role in various real-world applications, including medical imaging, automated inspection systems, and autonomous vehicle navigation, where precise edge detection is essential for accurate decision-making.

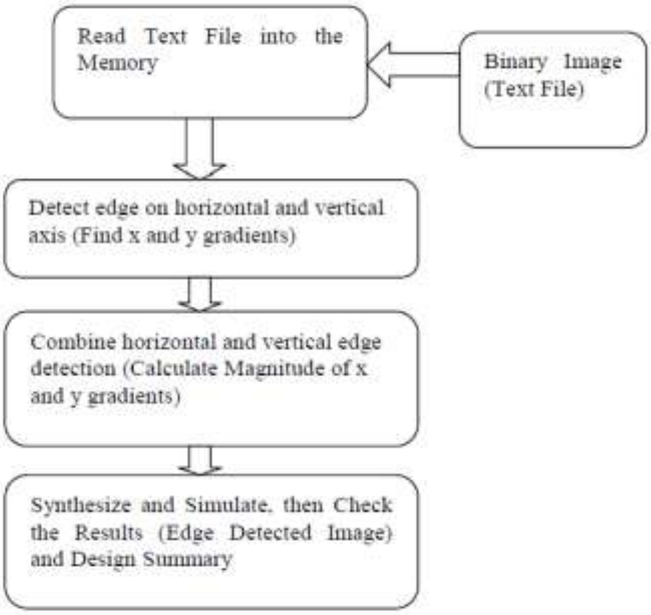

Read Text File into the Memory
Binary Image (Text File)
Detect edge on horizontal and vertical axis (Find x and y gradients)
Combine horizontal and vertical edge detection (Calculate Magnitude of x and y gradients)
Synthesize and Simulate, then Check the Results (Edge Detected Image) and Design Summary

Figure 12 VLSI PART (USING Modelsim)

XILINX ISE (INTEGRATED SYNTHESIS ENVIRONMENT)

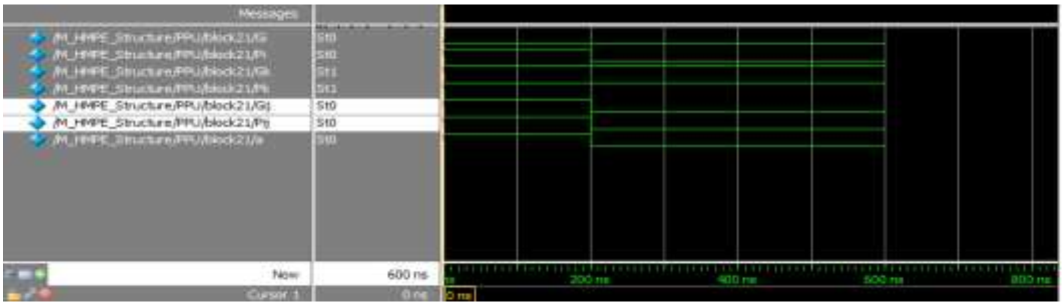
As part of the FPGA Targeted Design Platform approach, Xilinx has refined its tool flows to suit specific design disciplines. Xilinx now offers domain-specific editions of the ISE Design Suite to help users pair tools with specific jobs while managing costs effectively. One such edition is the DSP Edition, designed for algorithm developers and logic designers. Additionally, the Xilinx Software Development Kit (SDK) is available for users wanting to conduct application software development. The shift to Targeted Design Platforms has been beneficial for Xilinx, particularly during economic downturns. While the dot-com bubble in 2001 severely impacted the communications sector, Xilinx diversified its business across industries like aerospace, defense, automotive, industrial, and broadcasting. This diversification has reduced reliance on the communications sector, leading to greater resilience. A key trend influencing the FPGA market is the decline of ASICs. Due to increasing complexity and manufacturing costs, ASIC design starts have decreased significantly. FPGAs, with their flexibility and lower development costs, have become a preferred choice for companies needing to differentiate their products without the financial burden of ASIC development.

Xilinx's Targeted Design Platforms are categorized into three levels: the Base Platform, providing foundational tools and resources; the Domain-Specific Platform, tailored for specific user profiles like embedded processing developers, DSP developers, and logic/connectivity developers; and the Market-Specific Platform, designed for specific industries such as automotive, consumer electronics, military, communications, and ISM. The ISE Design Suite includes a robust set of design tools for various user profiles, from novice designers to experienced engineers. It offers enhancements such as faster compile times, improved simulation, and tailored optimization features for power, performance, or area. Key features include integrated tools for synthesis, simulation, and programming, faster place-and-route algorithms, and FLEXnet licensing for flexible usage tracking. MATLAB, developed by Cleve Moler in the late 1970s, is a powerful tool for numerical computation and data visualization. Widely used across engineering, physics, and data science fields, MATLAB provides built-in functions for tasks like signal processing, image analysis, and algorithm development. MATLAB 2014b introduced significant updates, including a new graphics system with enhanced rendering, improved matrix operations, and expanded support for parallel computing. Its enhanced user interface and expanded GPU capabilities made it particularly useful for applications in signal processing, image analysis, machine learning, control systems, financial modeling, and medical imaging. By leveraging the capabilities of both Xilinx ISE and MATLAB 2014b, engineers can accelerate product development, optimize designs, and ensure efficient, high-performance solutions across various industries.

SIMULATION IMPLEMENTATION

Black Ball

The waveform image represents the simulation output of a hardware design, showing signal transitions over time. The listed signals (Gi, Pi, Gk, Pk, Gj, Pij, a) belong to a module in M_HMPE_Structure/PPU/block21. The black ball (St0, St1) indicates logic states, where St0 = LOW (0) and St1 = HIGH (1). The transitions at 200 ns, 400 ns, and 600 ns reflect changes in the circuit's behavior, likely due to input processing or internal computations. This simulation helps verify the design, ensuring correct logic operation before hardware implementation.

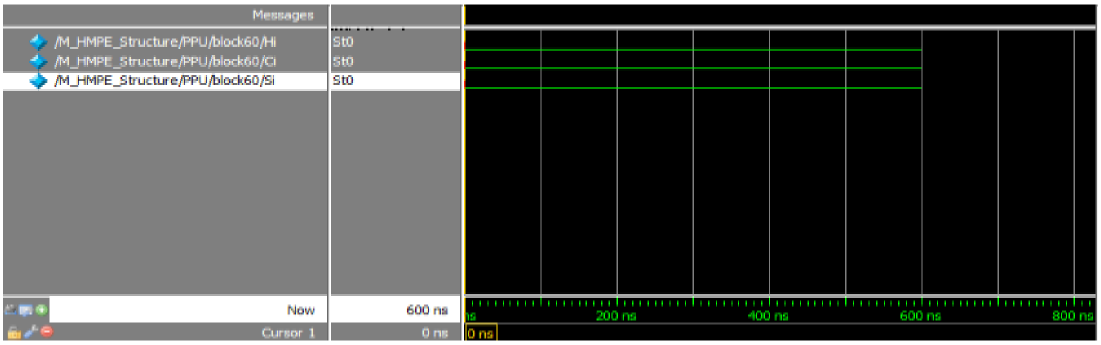


```
/M_HMPE_Structure/PPU/block21/Gi    St0
/M_HMPE_Structure/PPU/block21/Pi    St0
/M_HMPE_Structure/PPU/block21/Gk    St1
/M_HMPE_Structure/PPU/block21/Pk    St1
/M_HMPE_Structure/PPU/block21/Gij   St0
/M_HMPE_Structure/PPU/block21/Pij   St0
/M_HMPE_Structure/PPU/block21/a     St0
Now        600 ns
Cursor 1     0 ns
```

Figure 13 Black Ball

Diamond

The waveform image displays the simulation results of signals (Hi, Ci, Si) within M_HMPE_Structure/PPU/block60. The diamond symbols (St0) indicate that all signals remain in a steady LOW (0) state throughout the simulation period (0 ns to 800 ns). This suggests no significant transitions or changes in logic states, implying that the block might be in an idle state or waiting for an input trigger. The simulation helps verify the design’s behavior and ensures proper functionality before hardware implementation.



```
Messages
/M_HMPE_Structure/PPU/block60/Hi   St0
/M_HMPE_Structure/PPU/block60/Ci   St0
/M_HMPE_Structure/PPU/block60/Si   St0
Now        600 ns
Cursor 1   0 ns
```

Figure 14 Diamond

Parallel Prefix Unit

The waveform illustrates the output of the Parallel Prefix Unit (PPU), showing the computation of binary values based on input signals A, B, and S. The displayed binary sequences represent intermediate and final computational results at various time steps. The signals exhibit stable transitions, confirming correct bit-wise operations and propagation of values through the circuit. The PPU efficiently computes prefix operations, which are essential in fast addition techniques like carry-lookahead adders. The consistent bit patterns indicate proper functionality, validating the design before hardware implementation.

Figure 15 Parallel Prefix Unit

Application Result

Modelsim Simulation Result

The ModelSim simulation results display the waveform output for the given testbench, verifying the functionality of the design. The signals, including clock (clk), reset, start, and multiple data lines (m1, m2, etc.), exhibit expected transitions over time. The proper propagation of binary values and hexadecimal representations confirms correct logic execution. The presence of stable states and dynamic changes ensures that the system behaves as intended under various conditions. This simulation serves as a crucial step in validating the design before hardware implementation, ensuring accuracy and performance efficiency.

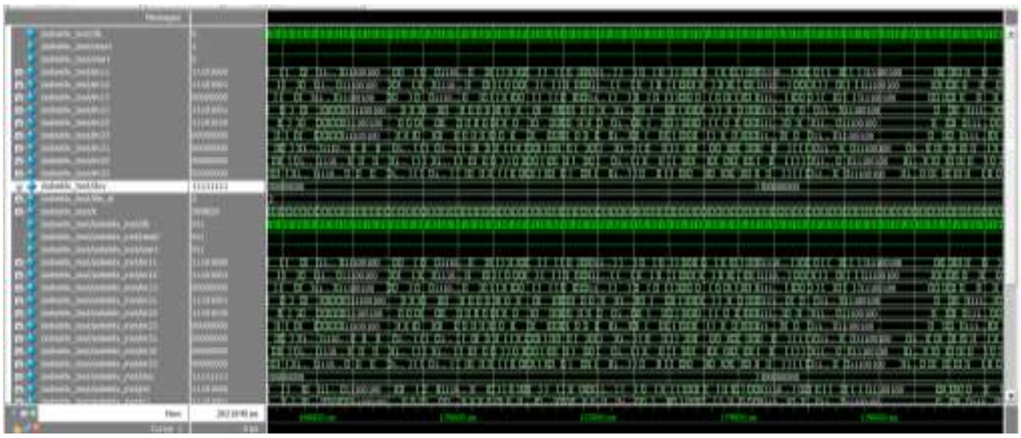


Figure 16 Modelsim Simulation Result

Matlab Result

Focuses on edge detection using quantum computing gates specifically the CNOT and Toffoli gates. These quantum operations were utilized to enhance the contrast at the edges of objects in the image, effectively detecting boundaries. The left figure represents the original grayscale image, while the right figure displays the processed output, where the edges of the four coins are distinctly highlighted against a black background. The application of quantum gates in image processing leverages quantum parallelism, potentially offering computational advantages over classical methods. This approach is significant for advancing quantum image processing techniques, demonstrating the feasibility of quantum computing in edge detection and object recognition.

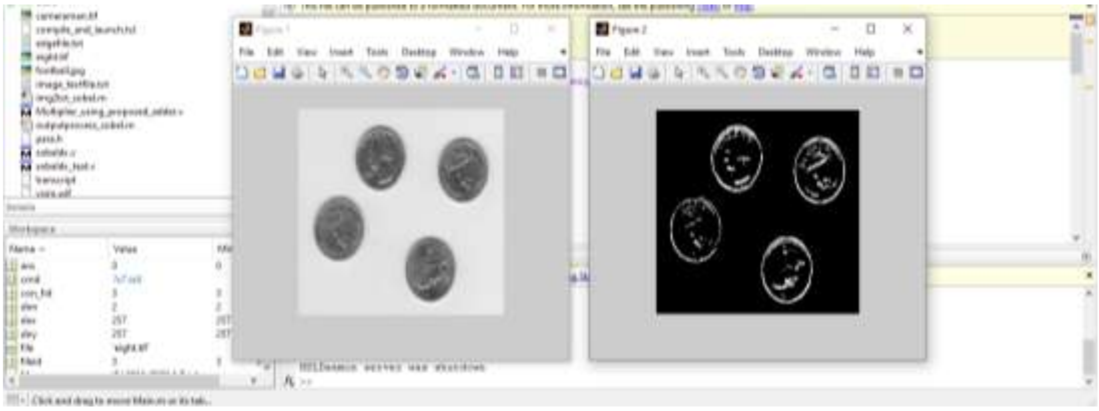


Figure 1
File Edit View Insert Tools Desktop Window Help
Figure 2
File Edit View Insert Tools Desktop Window Help
Workspace
Name
Value

Figure 17 Matlab Result

Proposed RTL Design

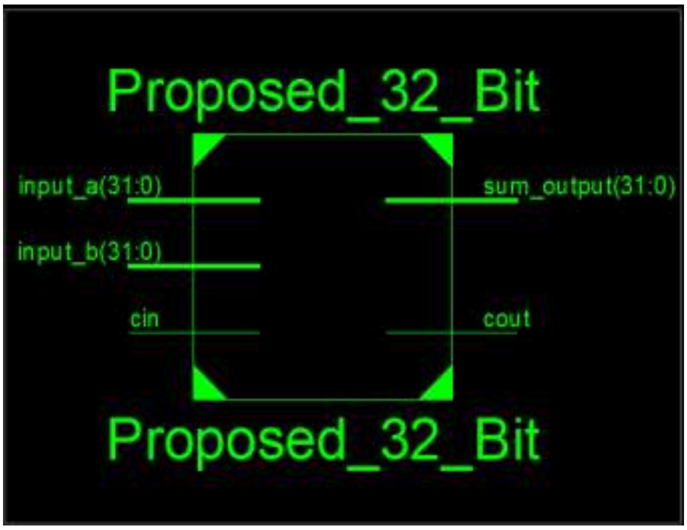


Figure 18 Proposed RTL Design

The image represents the RTL (Register Transfer Level) design of a proposed 32-bit arithmetic circuit, likely an adder. The design includes two 32-bit input operands, input_a(31:0) and input_b(31:0), along with a carry-in (cin). The circuit processes these inputs and produces a 32-bit sum output (sum_output(31:0)) and a carry-out (cout). The RTL representation visually demonstrates the data flow and interconnections within the design. This proposed 32-bit architecture is aimed at efficient arithmetic operations, potentially optimizing speed and power consumption for high-performance computing applications.

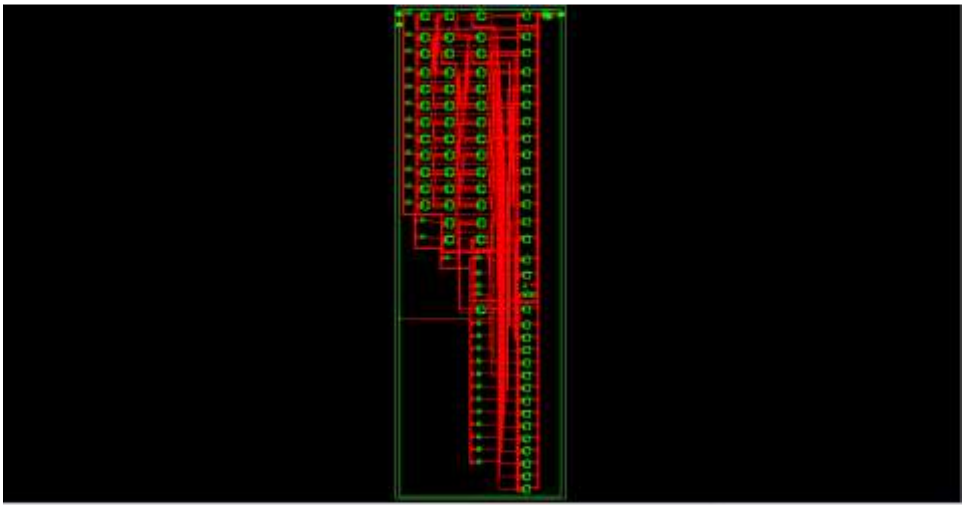


Figure 19 Internal Circuit of Proposed RTL Design

Technology Schematic

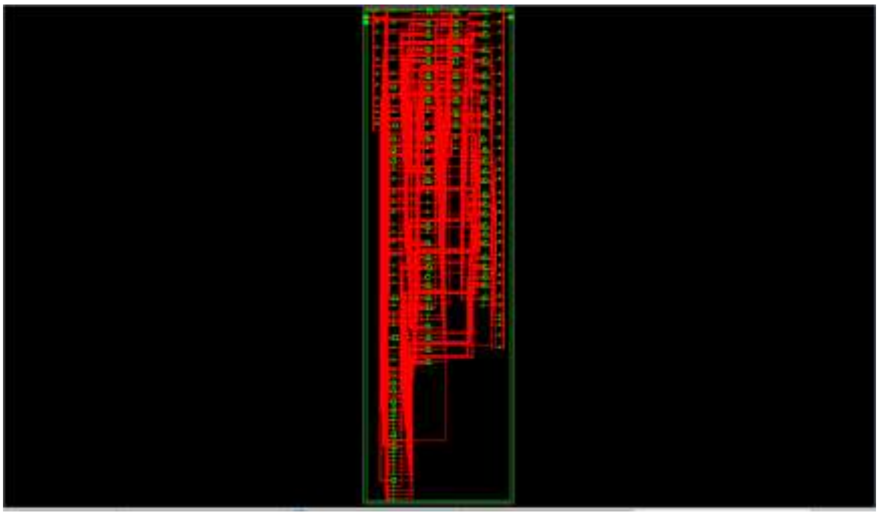
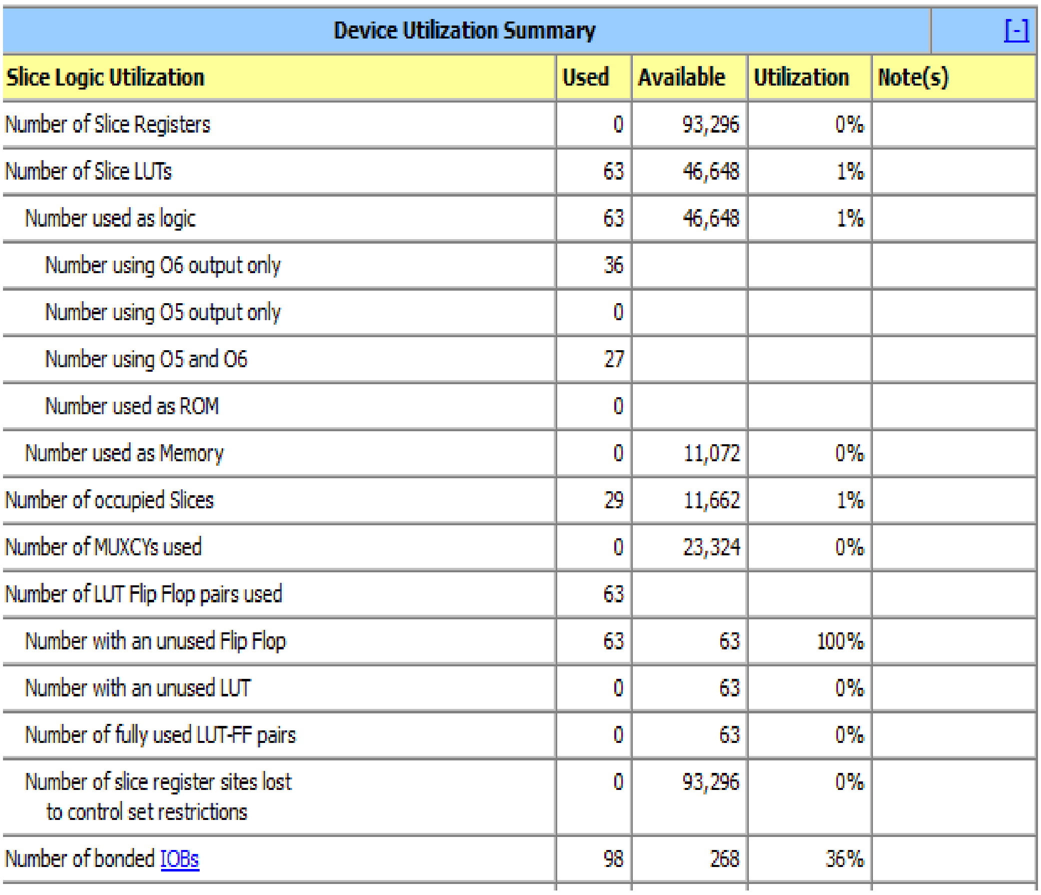


Figure 20 Technology Schematic

Device Utilization Summary

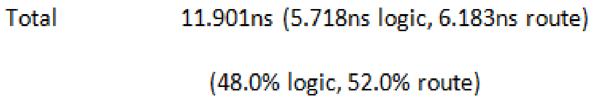
Conventional Modulo Adder

Table 3 Device Utilization Summary



Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	0	93,296	0%	
Number of Slice LUTs	63	46,648	1%	
Number used as logic	63	46,648	1%	
Number using O6 output only	36			
Number using O5 output only	0			
Number using O5 and O6	27			
Number used as ROM	0			
Number used as Memory	0	11,072	0%	
Number of occupied Slices	29	11,662	1%	
Number of MUXCYs used	0	23,324	0%	
Number of LUT Flip Flop pairs used	63			
Number with an unused Flip Flop	63	63	100%	
Number with an unused LUT	0	63	0%	
Number of fully used LUT-FF pairs	0	63	0%	
Number of slice register sites lost to control set restrictions	0	93,296	0%	
Number of bonded IOBs	98	268	36%	

Delay

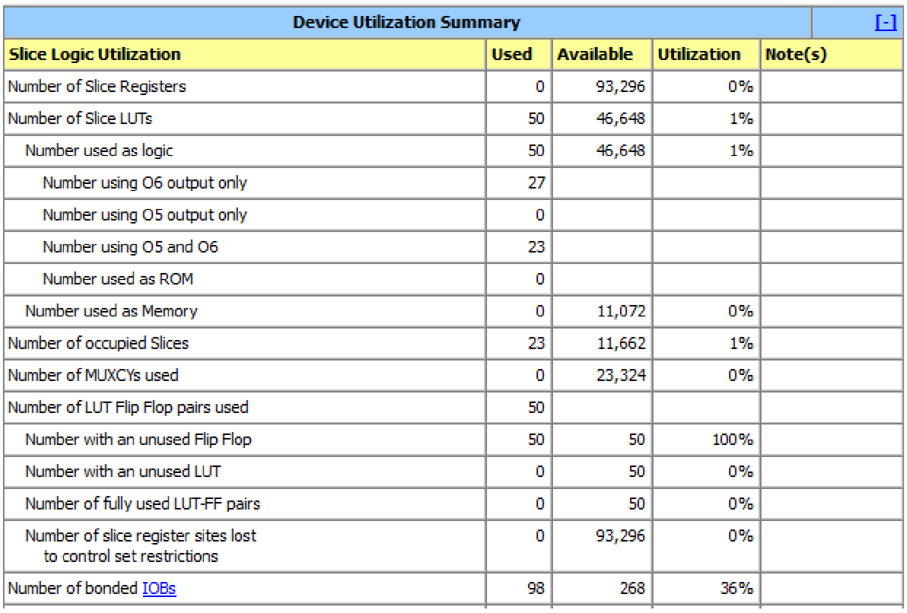


Total 11.901ns (5.718ns logic, 6.183ns route)

(48.0% logic, 52.0% route)

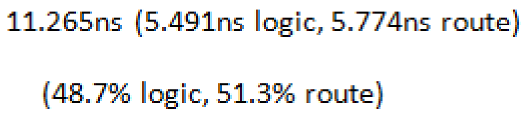
Proposed Modulo Adder

Table 4 Device Utilization Summary



Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	0	93,296	0%	
Number of Slice LUTs	50	46,648	1%	
Number used as logic	50	46,648	1%	
Number using O6 output only	27			
Number using O5 output only	0			
Number using O5 and O6	23			
Number used as ROM	0			
Number used as Memory	0	11,072	0%	
Number of occupied Slices	23	11,662	1%	
Number of MUXCYs used	0	23,324	0%	
Number of LUT Flip Flop pairs used	50			
Number with an unused Flip Flop	50	50	100%	
Number with an unused LUT	0	50	0%	
Number of fully used LUT-FF pairs	0	50	0%	
Number of slice register sites lost to control set restrictions	0	93,296	0%	
Number of bonded IOBs	98	268	36%	

Delay:



11.265ns (5.491ns logic, 5.774ns route)

(48.7% logic, 51.3% route)

Comparsision

Table 5 Comparsison Table

	Area			Delay		
Spartan 6 lx75t -2fgg884	**LUT**	**Slices**	**IOB**	**Overall Delay**	**Logic Delay**	**Route Delay**
Conventional Modulo Adder	63	29	98	11.901ns	5.718ns	6.183ns
Proposed Modulo Adder	50	23	98	11.265ns	5.491ns	5.774ns

The comparison table presents the performance metrics of the Conventional Modulo Adder and the Proposed Modulo Adder implemented on a Spartan-6 LX75T FPGA. The evaluation is based on key parameters such as the number of LUTs, slices, IOBs, and delay components. The Proposed Modulo Adder demonstrates improved efficiency by utilizing fewer LUTs (50 vs. 63) and slices (23 vs. 29), while maintaining the same number of IOBs

(98). Additionally, the overall delay of the proposed design is reduced to 11.265 ns, compared to 11.901 ns in the conventional approach. This improvement is attributed to a lower logic delay (5.491 ns vs. 5.718 ns) and route delay (5.774 ns vs. 6.183 ns).

These results indicate that the Proposed Modulo Adder offers better area optimization and faster computation, making it a more efficient alternative for FPGA-based arithmetic operations.

Area Grpah

The Area Graph compares the resource utilization of the Conventional Modulo Adder and the Proposed Modulo Adder in terms of LUTs, Slices, and IOBs. The proposed design shows a reduction in LUTs and Slices while maintaining the same number of IOBs, indicating better area efficiency. This improvement highlights the optimization achieved in the proposed design for FPGA-based arithmetic operations.

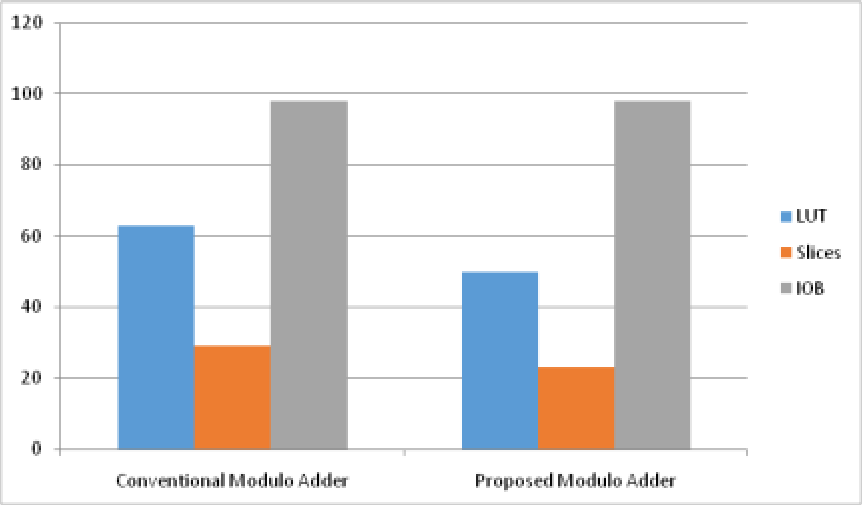


Figure 21 Area Graph

Delay Graph

The Delay Graph compares the Overall Delay, Gate Delay, and Path Delay of the Conventional Modulo Adder and the Proposed Modulo Adder. The proposed design exhibits a reduced overall delay, indicating improved performance. This reduction in delay enhances the speed and efficiency of arithmetic computations in FPGA-based systems.

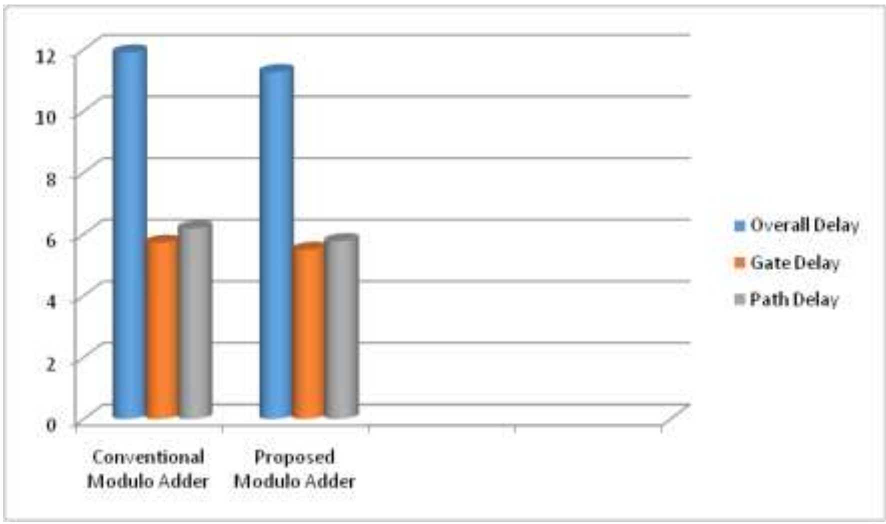


Figure 22 Delay Graph

CONCLUSION

The integration of quantum computing for edge detection offers a significant improvement in speed, accuracy, and computational efficiency compared to traditional methods. By utilizing quantum gates such as CNOT and Toffoli, the system processes images at a much faster rate. The incorporation of Modulo 2N+1 adders enhances the efficiency of arithmetic operations, reducing computational complexity. This optimization allows the system to handle larger datasets and perform complex calculations without overloading the hardware. The quantum-based edge detection system provides more precise results than classical algorithms, leading to better edge identification in images. This is crucial for applications in fields such as medical imaging and computer vision. The proposed system is scalable, making it suitable for large-scale, real-time image processing tasks. It can be applied to a wide range of industries, including video surveillance, robotics, and autonomous vehicles. As quantum computing continues to evolve, this project showcases how quantum techniques can enhance existing systems, making it a future-proof solution for edge detection and other image processing applications. This paves the way for more advanced, efficient, and reliable systems in the years to come.

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